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Design and Implementation of an ATM PON Slave Chip

Chan Kim
ETRI
ckim@etri.re.kr

Seung-Hwan Kim
ETRI
sammy@etri.re.kr

Tae-Whan Yoo
ETRI
twyoo@etri.re.kr

Abstract -- In ETRI, a PON physical layer chip-set was developed for the cost-effective accommodation of many residential subscribers with higher bandwidth needs. It has frame and message processing with ranging function. With a very short development time, it functions correctly with little bugs and it's being used in low-cost PON based access network system.

1. Introduction

As the telecom operator is trying to connect more subscribers to the network providing more bandwidth economically, the PON(passive optical network) is beginning to emerge as a practical solution. In ETRI, a PON physical layer chip-set was developed for the cost-effective accommodation of many residential subscribers with higher bandwidth needs. This paper describes the design and implementation of the PON slave chip that is under experiment with PON master chip.

2. ATM PON Standards

2.1 Network architecture

ITU-T recommendation G.983-1 describes a flexible optical fibre access network capable of supporting the bandwidth requirements of ISDN and B-ISDN services. The recommendation describes systems with nominal symmetrical line rates of 155.520 Mbit/s and asymmetrical line rates of 155.520 Mbit/s upstream and 622.080 Mbit/s downstream. The Recommendation proposes the physical layer requirements and

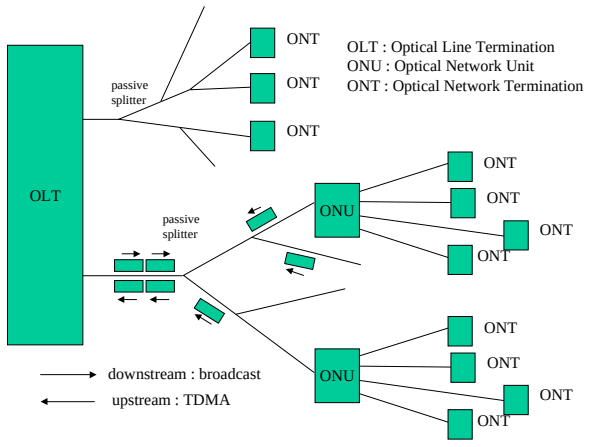

Figure. 1 PON-based access network

Figure 1 shows the PON-based access network

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specifications for the physical media dependent layer, the TC layer and the ranging protocol of an ATM-based Passive Optical Network (ATM-PON)
architecture. This system consists of optical line termination (OLT), optical network unit (ONU) and fibre cable in passive optical network (PON) configuration using passive optical splitter. One fibre is passively split between multiple ONUs who share the capacity of one fibre. Because of the passive splitting, special actions are required with respect to privacy and security. Moreover, in the upstream direction a TDMA protocol is required with special function called ranging to overcome the difference in propagation delay and processing latency of all the ONUs.

Table 1 shows the layered structure of ATM-PON network.

Table. 1 Layered Structure of ATM-PON Network

Path layer			Refer to I.732
Trans-mission medium layer (with related OAM functions)	TC layer	Adaptation	Refer to I.732
		PON transmission	Ranging Cell slot allocation Bandwidth allocation Privacy and security Frame alignment Burst synchronization Bit/byte synchronization
	Physical medium layer		E/O adaptation WDM Fibre connection

2.2 Transmission Convergence Layer

Transport Specific TC functions

The PON master-slave chip handles the function of TC layer. The downstream bit rate is 622Mbps or 155Mbps and upstream rate is 155Mbps. Figure 2 shows the frame format for the 622Mbps downstream and 155Mbps upstream data.

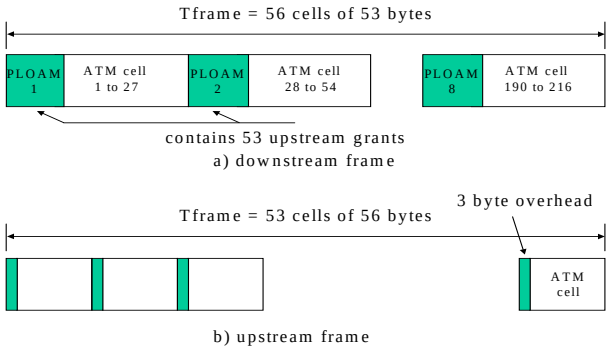

Figure 2. Frame format for 622.08/155.52 Mb/s PON

Downstream frame consists of 4*56 cells and PLOAM cells are inserted every 28 cells for management of the link. The downstream cell format, HEC, cell delineation, distributed sample scrambler's operation, idle cell and PLOAM cell pattern are described in the recommendations. The downstream PLOAM cell has in its payload, some control fields, grant values with CRC for groups of 7 or 6 grant values. It also carries the message with CRC from the master directed to a specific ONU or broadcast and BIP code for error monitoring. The grant values represent which ONU can use the corresponding upstream slot for which kind of cell(data, PLOAM, ranging,...) .

In upstream, the cell is 56 byte long with 3 byte overhead. The cell delineation is done by ranging procedure for each ONU with TDM slot assignment using downstream grant values. The upstream cells or mini-slot cells are also scrambled with cell synchronous scrambler. The idle cell and PLOAM cell format is defined in the recommendation. The upstream PLOAM cell has some control fields, message with CRC, and LCF (laser control field), RXCF (receiver control field), and BIP value for error monitoring purpose.

The OLT and ONU have OAM procedures for fault and performance monitoring. The OLT manages major alarms like LOS, LCD, CPE, OAML, DACT for each ONU. The ONU manages cell, PLOAM cell, and Frame sync state as specified in the document.

For its inherent downstream broadcast signal, to prevent any ONU from listening to other ONU's data at the downstream, a special method called churning is used. Each ONU generates and sends its churning key to the OLT. The master uses different churning key for each ONU data for churning enabled connections. The churning key is changed periodically for each ONU with OLT's request and ONU's response and with a synchronization mechanism.

There are many messages downstream and upstream for the previously mentioned ranging, churning and OAM procedures or authentication but the details will not be discussed here.

2.3 Ranging Method

Ranging is an important procedure in the PON system because the upstream fiber is shared by multiple ONU systems using TDMA method. Since each ONU has different length from the OLT system, and the difference can be thousands of upstream clock periods apart, the OLT assigns each ONU arbitrary delay values in unit of upstream bits to make all the ONUs look as if they are at the same distance.

Figure 3 shows the timing reference of OLT and ONU. Through ranging process, all the timing variation in the ONU systems are absorbed and eliminated to make them have equal round-trip delay in the OLT's point of view. This ranging process is initiated periodically for a newly powered-on ONU or by an operator. Fine ranging can be performed during operation. The ranging starts with assigning upstream overhead and then the PON ID, grant values for each ONU are assigned. Then delay measurements is done by measuring the time until the upstream ranging cell is received for a downstream ranging grant. When the delay is measurement is successful, the OLT assigns the required additional delay Td for the ONU to make the round-trip delay to be equal to a predefined value. When the Td value is assigned, the ONU enters the operating state.

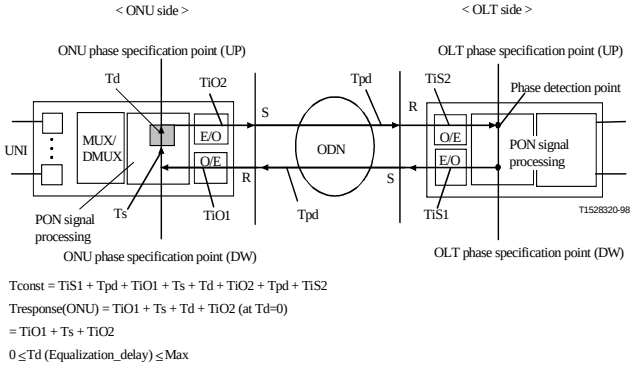

Figure 3. timing reference for ranging

3. ASIC Architecture and Implementation

3.1 Main schemes of the chip

Implementing the controller

Since the PON slave chip is processing frames, the control parts have in its center cascaded counters to decode timing information. Figure. 4 shows the phase relationship of the downstream and upstream frame at the slave R/S point.

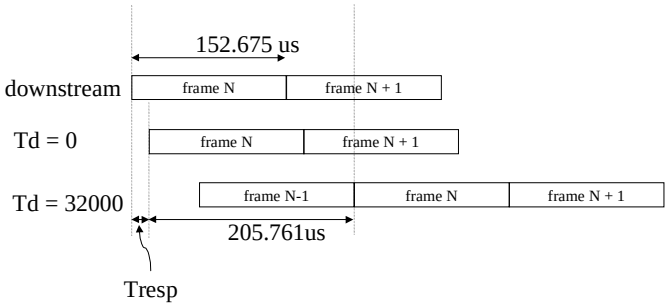

Figure 4. Frame phase relationship

Since the downstream frame consists of 56 of 53 byte cells, the receiver should have 56 x 53 counter structure. But to differentiate the corresponding frames which can be offset by greater than a frame period, another 2 bit counter is used to identify adjacent frames and it becomes 2 x 56 x 53. In the same way, the upstream counters are composed of 2 x 53 x 56 since upstream frame is composed of 53 slots of 56 byte long cell.

When ranging time message is received, the slave chip applies more time delay to the prior phase difference between the receive frame counter and transmit frame counter. By letting the upstream counters start at the specified offset controlled by the delay value, the slave chip makes the upstream frame be more delayed as much as set by the ranging time delay value. During the delay measurement period in the ranging, when sending a ranging cell, the slave chip uses normal procedure of using allocated slot so that the Ts value

can be included in the ranging and absorbed out.

Applying the Td value during ranging

As said, the upstream frame counter's phase is shifted from that of downstream. Since the Td value is expressed in number of upstream bits, the value is divided by 8 and applied when placing the required byte off-set in the ASIC, and the remaining 0 ~ 7 bit delay(expressed in the lowest 3 bits of the Td) is further applied just before the data is output by shifting the data in the byte stream domain. By putting a programmable default delay, the Tresponse requirement is met.

Figure. 5 shows the method of adjusting the upstream frame phase with respect to the downstream frame. The rx frame counter and tx frame counter have frame count(0~3) as well as slot and byte count. The rx frame sync pulse is delayed and used to synchronize the upstream frame counters. When synchronizing the upstream frame counter, the first 2 bits indicating the 0,1,2,3,0,1,.. frame sequence is also copied so that the frame correspondence is also set up. The phase aligning is applied every two frame.

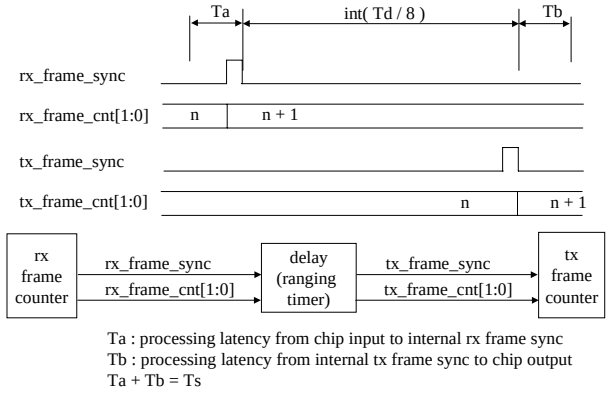

Figure 5. Upstream frame counter synchronization according to the raning timer delay

Storing and reading grant values

In the downstream block, it decodes the received grant values by comparing it with the assigned grant values and keeps the result in the grant table (It saves some gate counts to use decoded form). The 2 bit frame counter value is also used to address the location to keep the decoded grant value and the 2 bit frame counter value is also used in the transmit side with slot counter to decode whether to send a cell or which kind of cell to send. Therefore, the slot correspondence is maintained across phase difference greater than two frame time.

The decoded value is summarized into 5 values.

① My Data Grant
② My PLOAM Grant
③ My Divided Slot Grant
④ Ranging Grant
⑤ Disabled (Reserved, Unassigned, other ONUs')

When CRC error occurs, the corresponding block of grant table is indicated to be invalid using separate bit. The slot decoding part reads the grant table and generates the corresponding start pulse for each selected cell type to send. All the action in the cell generation part is dependent on the cell start pulses.

Operation of the state machine for Ranging

A state machine is operated in the slave according to the G.983.1 specification. The state machine changes the state when specific event is detected in each state and all the cell/message reception and transmission is dependent on the current ranging state. For example, sending data cell is done only in the operating state(O8) and the sending PLOAM cell with serial number ONU message is done in O7 state when having received the PLOAM grant. Most of the events come from the receiver message processor.

3.2 Block Diagram and Functions of Each block

Figure 6 shows the block diagram of the PON slave controller with all the functions explained above.

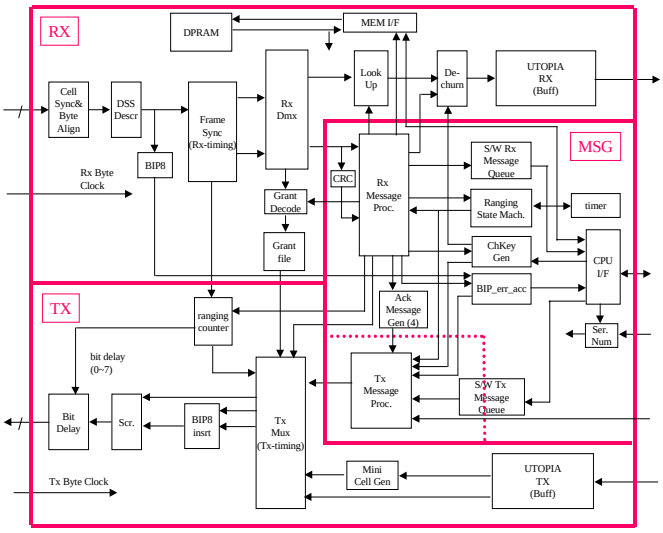

Figure 6. Block diagram of the PON Slave ASIC

3.2.1 RX processing block (RPB)

The CD(Cell Delineation) seeks for the cell boundary for 8 possible byte allignments and if a cell boundary is discovered, declare it as the correct byte and cell boundary(Figure.7). The cell delineation has HUNT, PRESYNC, SYNC state for each byte stream. The upper most two bits are excluded in the HEC verification until the RX descrambler is synchonized to the cell stream. The result is the cell stream.

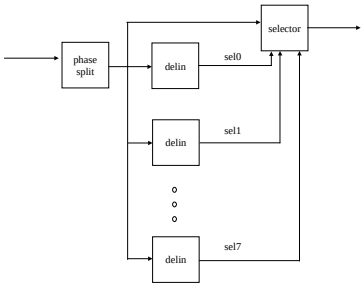

Figure 7. Cell and Byte Delineation

The DSCR adds the two bit samples to its PRBS generator and synchronize the PRBS to that of the transmitter. It has acquisition, verification and steady state.

FD(Frame Detect) sees the ATM cell stream and identifies the periodic PLOAM cell location(PLOAM synch). After that, it inspects the IDENT bit of the PLOAM cell payload and detects the frame boundary. It lets out the byte stream with all the timing pulses as shown in Figure 8.

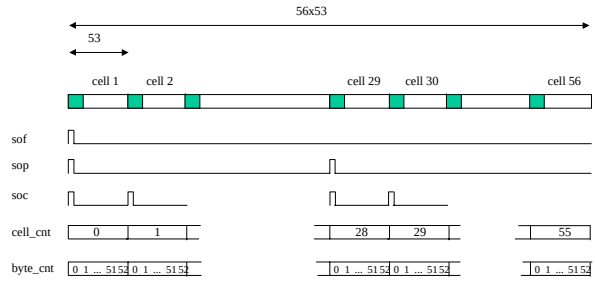

Figure 8. Receiver Frame Counter Timing Signal

BIP8 block detects BIP errors every PLOAM cell and the errors are accumulated and reported using interrupt. As set by the downstream BIP interval message, the value is periodically passed to the TX message processing block and sent upward as remote error message.

RX_DMUX block extracts each part of the PLOAM and data cell and sends them to either LOOKUP block or GNT_DCD.

Grant_DCD decodes the received grant values and writes them to the grant table as explained before for transmiter's use.

The Lookup block extracts the VPI and looks up the corresponding table entry to knows out whether to receive the cell or not and whether to dechurn it or not.

The block has internal 4K entry DPRAM to keep the setting for 2^12 VPI values. Since not only the lookup block but also the CPU block, and the receive message processor(to process the churned VP message) access the DPRAM, a memory arbiter arbitrates the DPRAM access. With the possible arbitration latency, 10 clock cycle was assigned as enough time to get the table data for normal lookup. The writing and reading from the CPU is indirectly done through special data and address register and triggering mechanism. The CPU should check a flag for the access completion.

Dechurning block de-churns the cell payload in case it is marked to be churned. Each time the churnking key update message is received, the internal frame count is set to 48, 32 or 16 according to the message count and decremented each frame to synchronize the churning key update.

The UOTPIA_RX block saves the cell in its buffer and lets it out when read from outside.

3.2.2 TX processing block

UTOPIA_TX block receives ATM cells from the UTOPIA I/F and stores them in the FIFO. When the cell enable is coming from the TX MUX, it reads the cell from the FIFO and sends it to the TX_MUX or sends idle cell when there is no ATM cell in the FIFO.

TXTIME controls the entire transmit block and generates 53 pulses with interval of 56 supplying the counter value for other parts to decode the timing. The signal generated in the TXTIME look like that in Figure 9. (TXTIME is internal to the TXMUX)

TX_MUX sends the cell or message enable signal to the TX_UTOPIA or TX messgae processing block for each slot according to the grant table value assigned to the slot. Whan in ranging state O5 and received ranging grant or in O7 and received PLOAM grant, a ranging cell should be sent. In this case, with the message enable, a special signal is used to indicate that a ranging cell(serial number ONU message) should be sent.

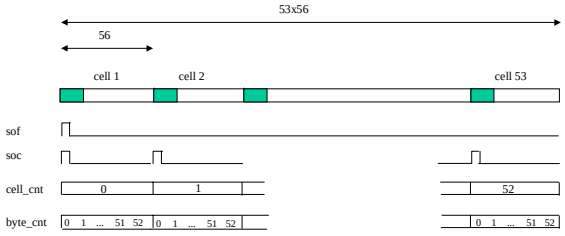

Figure 9. Transmit timing signals

It selects these data and overhead to form actual output cell. For example, in case it is a data cell for a slot, the tx_mux selects the overhead, and ATM cell coming from the UTOPIA/FIFO block. When a PLOAM cell should be sent, it muxes overhead, PLOAM cell header, IDENT pattern, and the message coming from the TX message processor, LCF, RXCF as the upstream PLOAM cell format.

3.2.3 MSG processing block

In PON system, the messages are transported up and downstream in the PLOAM cell payload. The message has PON_ID, message ID and 10 message field bytes.

The state machine in the RX part receives and interpretes the message from the start of the message and triggers small blocks for specific message type. According to the message type, they set registers, trigger other processing blocks with paramters or write the message to the receive message buffer for CPU processing. About 20 types of messages are processed at the downstream mostly for ranging, OAM, churning, ATM layer. For example, when the churning key update message is received, the number of frames until the key changing frame is passed to the de-churning part.(It already has the key to use next time). Likely, if churning key request message is received, the message processing block lets the tx message processing block know this and the block receives a new key from the key generator and sends the new churning key message three times. When grant allocation message is received, it sends the grant values to the GNT_DCD block.

The TX message processing block forms and delivers message when the enable signal is coming from the tx_mux block. The message to generate is determined by the pending requests for each message generation. The CRC value is inserted later at the tx_mux block. About 10 types of messages are processed at the upstream for ranging, OAM, churning and acknowledgements.

Pending message send requests are served with priority and, for messages to be sent multiple times, specific counters are set and decremented until it is done. For equal priority, cyclic

service is applied.

For acknowledge messsages, the received message is saved in each acknowledge FIFO and the request is set for the acknowledgement and serviced. Since there are several types of acknowledge message with different priority, there should be separate acknowledge FIFO.

4. Top Simulation

It is very important to verfiy the functional behavior of an ASIC using realistic simulation. For this ASIC, a testbench was written without the master chip to test the slave chip's behavior and later master-slave co-simulation was performed to correct more bugs and verify the functions.

4. 1 PON Slave-Only Simulation

Figure 10 shows the testbench of PON slave-only simualtion.

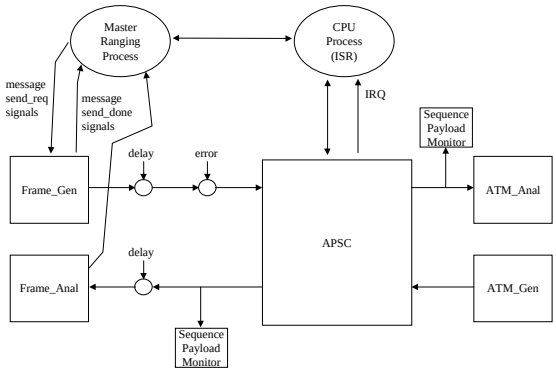

Figure 10. Simulation of APSC chip

To simulate the PON slave chip's functional behavior, cell_gen and cell_get entity was written to immitate the PON master behavior by generating the downstream traffic and analyzing the upstream traffic.

Cell_Gen generates downstream frame data according to 155 or 622 mode. It generates and multiplexes four different ATM traffic with different header, sequence number and payload pattern. For PLOAM cell, it generates the requested message with optional input data and sends it downstream on the PLOAM cell. It can generate all kinds of messages in the specification and has request-done handshaking interface. It is a complete transmitter having HEC, BIP, CRC generation and DSS scrambling funciton.

Cell_Get has upstream FSS descrambler, HEC verification, and notifies any ranging-related events to the ranging state machine. It displays the received cells header, message.

As shown in the Figure 11, the testbench has ATM processes which reads and writes ATM cells from/to the chip across UTOPIA-II interface. The monitoring of each connection's sequence number and payload was done outside using a montor. By this means, any error or bug in the final cell stream is easily discovered and corrected.

The CPU process in the testbench initializes the APSC chip and processes the interrupt request using polling method for convenience. The ISR(interrupt service routine) displays the cause of interrupt and any other releavant information on the simulator's window.

The process governing the ranging mimics the OLT's behavior for a set of predefined ranging methods. Since the cell_gen and cell_get have necessary interface with the ranging state machine, the whole testbench is run as scheduled for a defined ranging method.

Fig. 11 shows the defined ranging scenarios with the states. The actual testbench has more states to incorporate variation on the scenario and other functionalities other than ranging. (After the ranging is complete, the machine jumps back and forth to other states to test various message processing sequences)

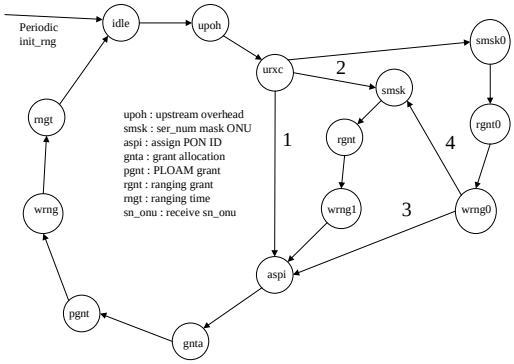

Figure 11. state diagram of the ranging process

The statemachine sends messages as set by the scenario so that the slave can jump up the states to normal O8 state. There are some variations in the ranging procedure related to optical power setup or serial number masking. The detailed procedure will not be explained.

All the messages including ranging, connection setup, churning, alarm processing were verified using specific senarios. Later in the project, the whole operation of ranging, data transport were verified together with the master chip(APMC).

5. Conclusion

At the time of this writing, most of the basic functions were verfied to be correct with master-slave experiment in the laboratory. The ranging, grant processing were tested and actual cell transmission up and down stream should be tested with setup procedure at the ATM layer and test equipement.

This slave chip was developed in 5 months but functions well and it will be integrated with ATM layer and VDSL function to implement single-chip ONU controller.

Reference

1. ITU-T Recommendation G.983-1 "Broadband Optical Access Systems Based on Passive Optical Networks(PON)"